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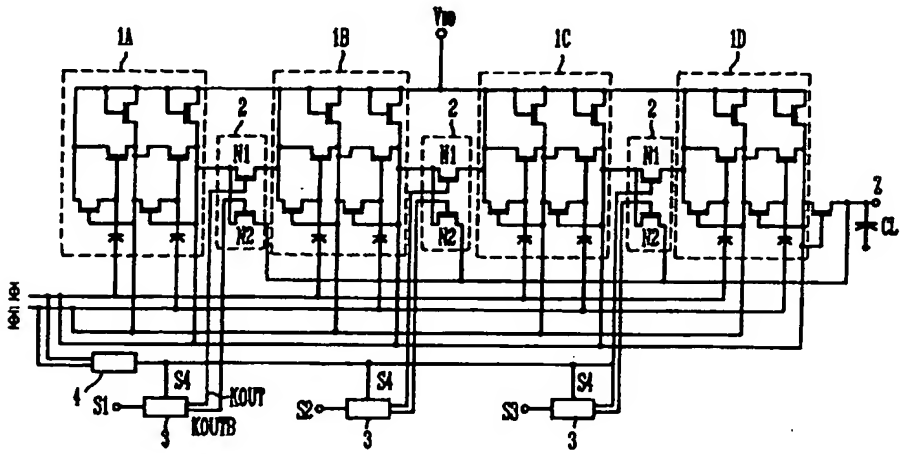
(54) **Charge pump circuit**

(57) In a charge pump circuit, which can perform high pumping by changing the condition of connections of unit charge pumps 1A, 1B, 1C, 1D, a series and parallel switching circuit 2 is connected between the unit charge pumps so that the output of one unit charge pump is connected to the input or output of the next unit charge pump or to the output of the charge pump circuit. The switching circuits 2 are controlled by a level shift circuit 3 which is described in detail (Fig 5).

FIG. 3



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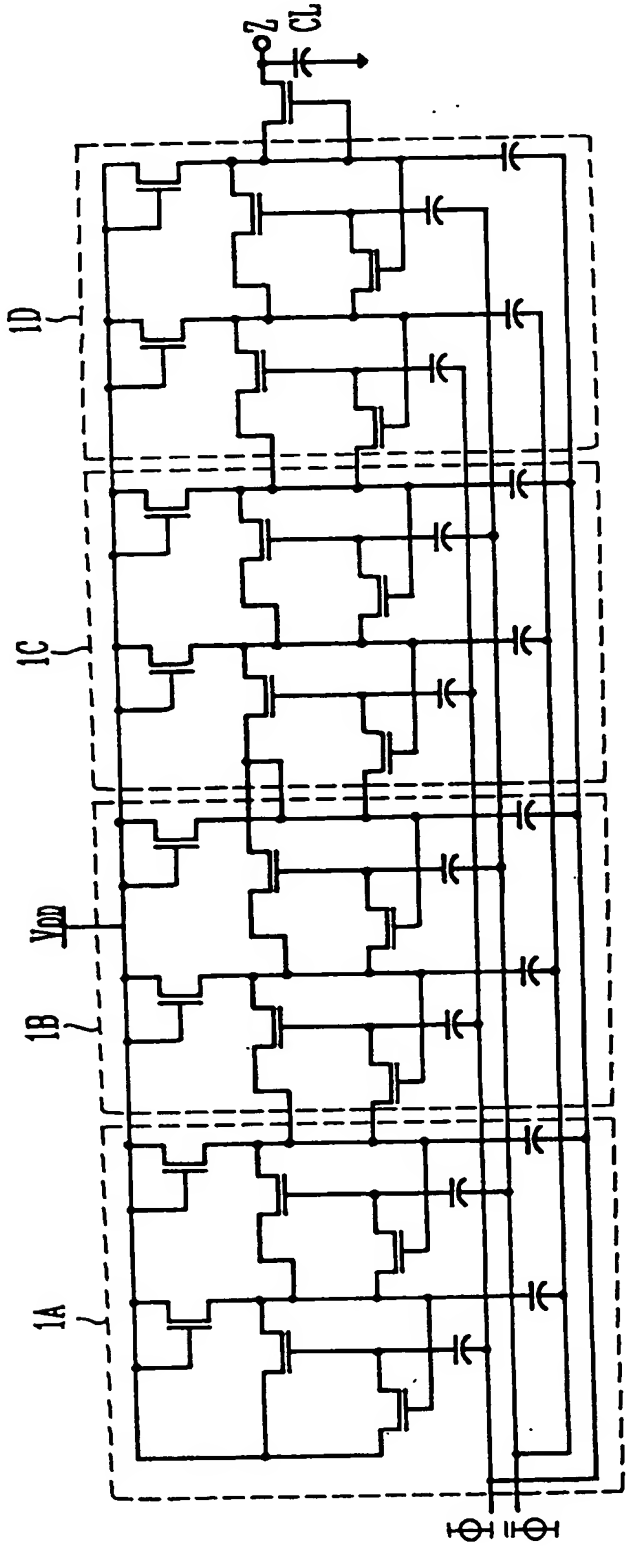

FIG. 1(PRIOR ART)

FIG. 2
(PRIOR ART)

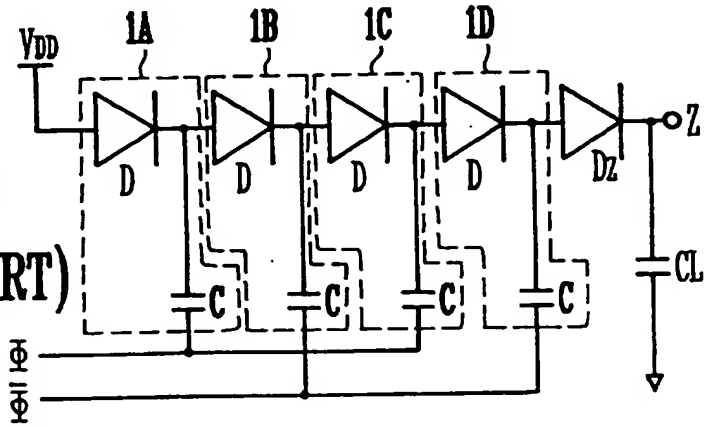

FIG. 4A

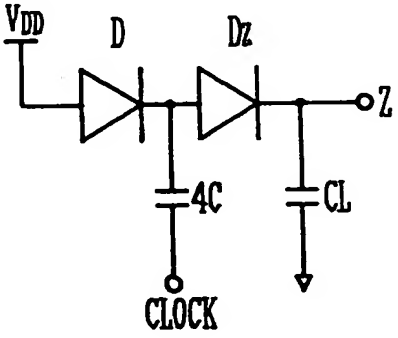

FIG. 4B

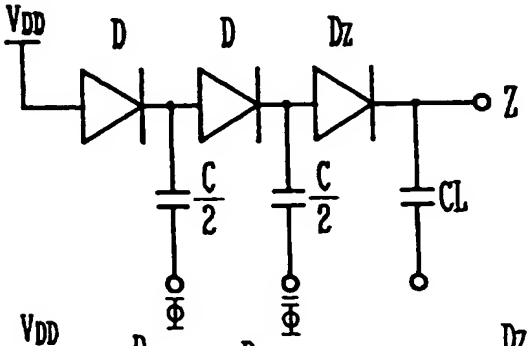

FIG. 4C

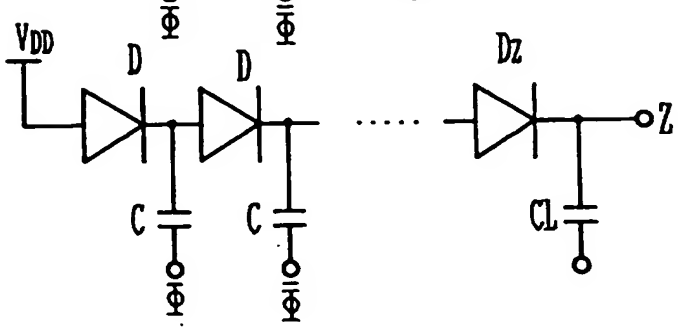

FIG. 3

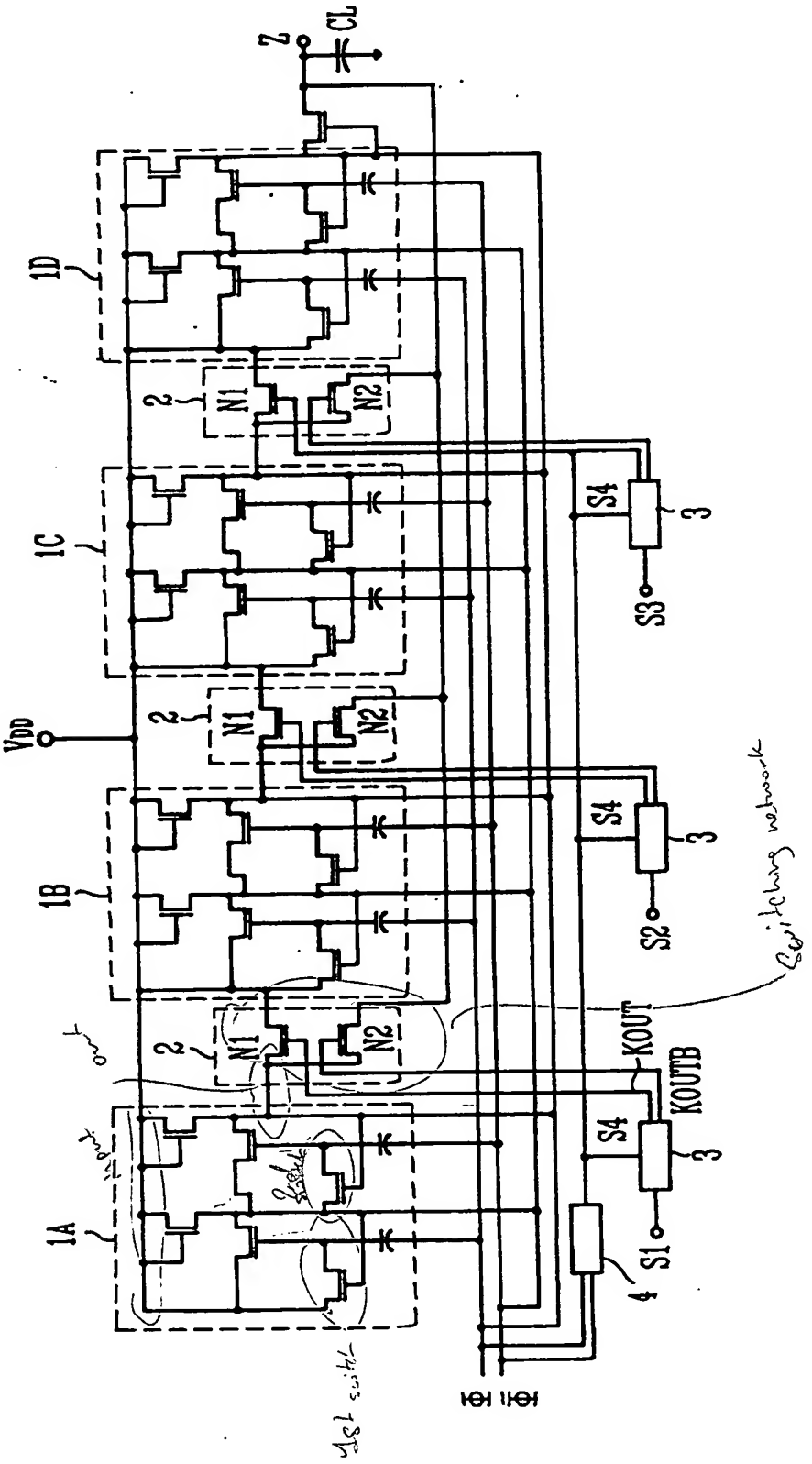

FIG. 5

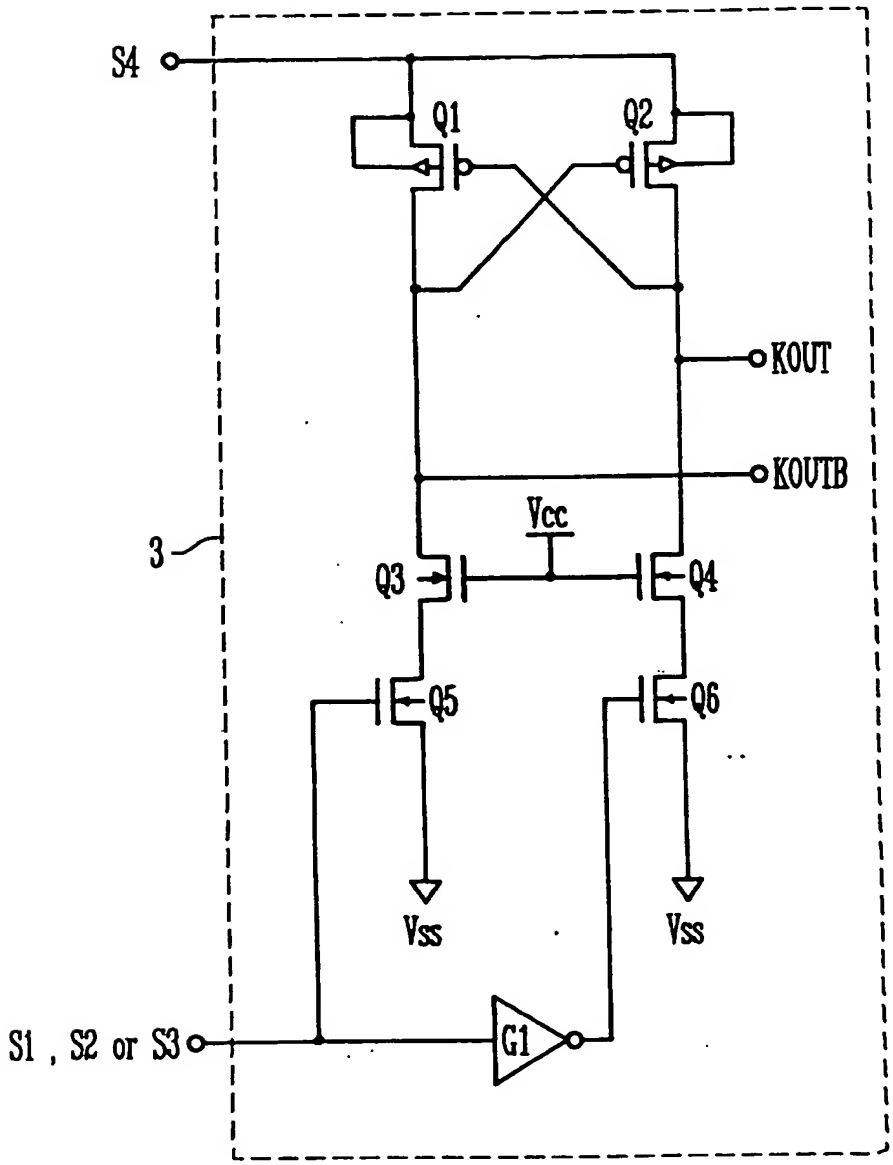

FIG. 6A

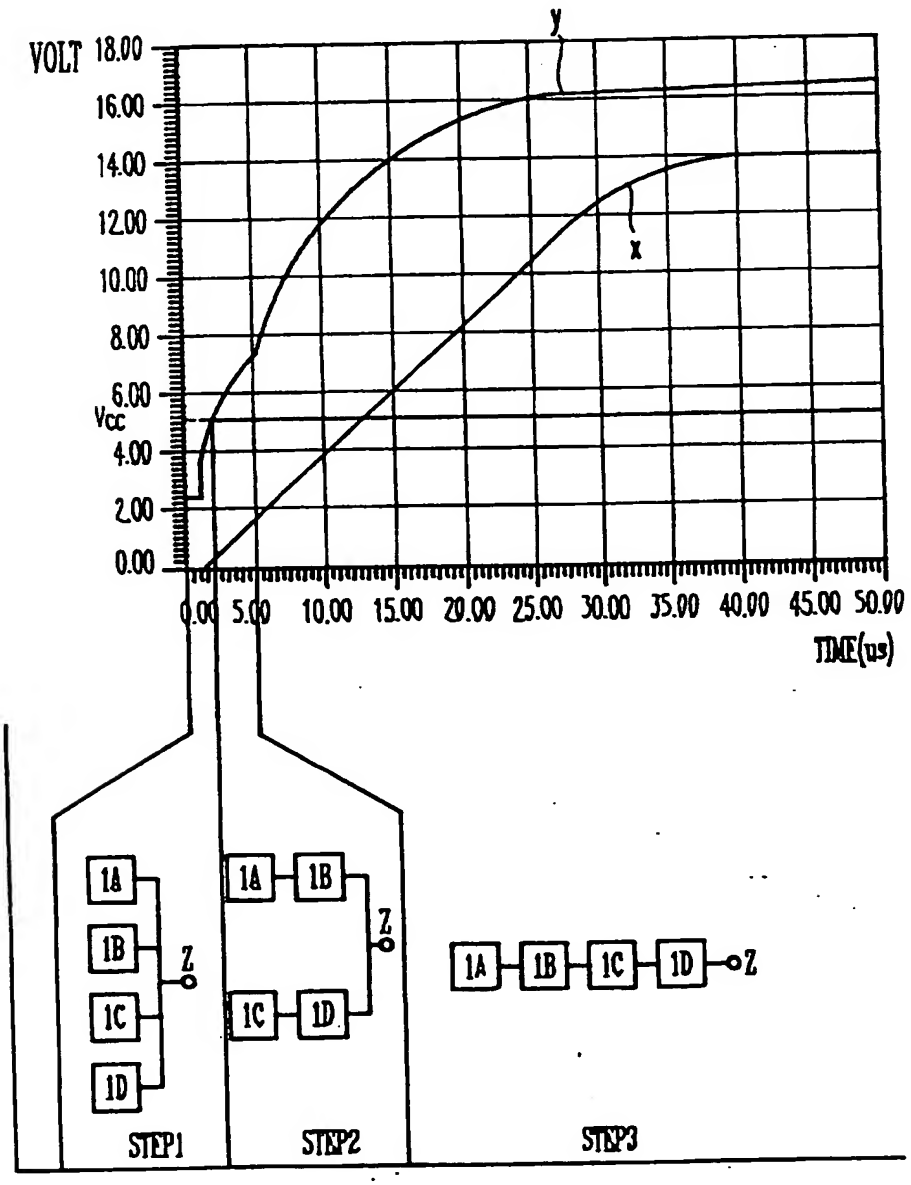
VOLT
18.00
16.00
14.00
12.00
10.00
8.00
6.00
Vcc
4.00
2.00
0.00
y
x
0.00 5.00 10.00 15.00 20.00 25.00 30.00 35.00 40.00 45.00 50.00
TIME(us)
1A
1B
1C
1D
Z
STEP1
STEP2
STEP3

FIG. 6B

CHARGE PUMP CIRCUIT

BACKGROUND OF INVENTION

Field of the Invention

The present invention relates to a charge pump circuit and, more particularly, a charge pump circuit which can reduce pumping time.

Information Disclosure Statement

As shown in FIG. 1, in a conventional charge pump circuit, a plurality of unit charge pump circuits 1A, 1B, 1C and 1D are connected in series between a supply power source VDD and an output terminal Z. Therefore, the supply power source VDD is charged up at each unit charge pump 1A, 1B, 1C and 1D in accordance with a two(2)-phase clock signals; Φ, $\overline{\Phi}$ and transferred to the output terminal Z.

FIG. 2 is an equivalent circuit for illustration of FIG. 1. As shown in FIG. 2, each unit charge pump 1A, 1B, 1C and 1D comprises a capacitor C and a diode D for charge pumping. Such unit charge pumps 1A, 1B, 1C and 1D are connected in series between the supply power source VDD and an output terminal Z. The supply power source VDD is charged up at each unit charge pump 1A, 1B, 1C and 1D in accordance with the two(2)-phase clock signals Φ, $\overline{\Phi}$ and transferred to the output terminal Z through a diode Dz. CL denotes a load capacitor in both FIGS. 1 and 2.

However, such conventional charge pump circuit has a disadvantage in that a consumption power is high and a charge

transfer efficiency at initial operation is lowered since the unit charge pumps are connected in series between the supply power source and the output terminal.

Summary of the Invention

An object of the invention is to provide a charge pump circuit which can solve the above advantage by connecting serial and parallel switching circuits between unit charge pumps and by controlling the serial and parallel switching circuits with a level shift circuit.

To achieve the above object, a charge pump circuit according to the present invention, comprises: a first unit charge pump connected to a supply power source and performing a pumping operation according to clock signals; a second unit charge pump connected to the supply power source and performing a pumping operation according to the clock signals; and a serial and parallel switching circuit for selectively transferring an output of the first unit charge pump to an input or output of the second unit charge pump according to a control signal.

BRIEF DESCRIPTION OF THE DRAWINGS

For fuller understanding of the nature and objects of the invention, reference should be had to the following detailed description taken in conjunction with the accompanying drawings in which:

FIG. 1 shows a conventional charge pump circuit;

FIG. 2 is an equivalent circuit for illustration of FIG. 1;

FIG. 3 is a charge pump circuit of the present invention;

FIGS. 4A through 4C are equivalent circuits for illustration of FIG. 3;

FIG. 5 is a detailed circuit of a level shift circuit of FIG. 3;

FIG. 6A is a graph for comparing an output of the conventional charge pump circuit and an output of the charge pump circuit of the present invention; and

FIG. 6B is a schematic diagram for illustration of FIG. 6A.

Similar reference characters refer to similar parts through the several views of the drawings.

DETAILED DESCRIPTION OF THE INVENTION

A detailed description of an embodiment of the present invention is given below with reference to the accompanying drawings.

FIG. 3 is a charge pump circuit of the present invention. Circuits of first, second, third and fourth unit charge pumps 1A, 1B, 1C and 1D are identical to the circuit of FIG. 1. A serial and parallel switching circuit 2 is provided between the first and second unit charge pumps 1A and 1B. The serial and parallel switching circuit 2 is connected to the first and second unit charge pump 1A and 1B and the output terminal Z. Each serial and parallel switching circuit 2 is also connected between the second and third unit charge pumps 1B and 1C and between the third and fourth unit charge pumps 1C and 1D, and also connected to the output terminal Z. The serial and parallel switching circuit 2 has two transistors N1 and N2. The transistor N1 is connected between the first and second unit charge pumps 1A and 1B. The

transistor N2 is connected to the first unit charge pump 1A and the output terminal Z. The transistor N1 and N2 between the second and third unit charge pumps 1B and 1C, and the transistor N1 and N2 between the third and fourth unit charge pumps 1C and 1D are connected in the same way as the transistor N1 and N2 between the first and second unit charge pumps 1A and 1B.

The serial and parallel switching circuit 2 is controlled by the level shift circuit 3. That is, the transistors N1 and N2 are turned on or off according to outputs KOUT and KOUTB of the level shift circuit 3. The level shift circuit 3 produces outputs KOUT and KOUTB according to each control signal S1, S2 or S3 and an output signal S4 of an auxiliary charge pump circuit 4 which is operated according to the two(2)-phase clock signal Φ, $\overline{\Phi}$. The reference number CL denotes a load capacitor. If the transistors N1 are turned on and the transistors N2 are turned off, the first through fourth unit charge pumps 1A through 1D are serially connected between the supply power source VDD and the output terminal Z. To the contrary, if the transistors N1 are turned off and the transistors N2 are turned on, the first through fourth unit charge pumps 1A through 1D are parallely connected between the supply power source VDD and the output terminal Z.

FIGS. 4A, 4B and 4C are equivalent circuits for illustration of FIG. 3. FIG. 4A can be regarded as an equivalent circuit of FIG. 3 in the condition that all the transistors N1 are turned off and all the transistors N2 are turned on. Therefore, the supply power source VDD is transferred to the output through a diode D and Dz. The resultant capacitance is 4C.

FIG. 4C can be regarded as an equivalent circuit of FIG. 3 in the condition that all the transistors N1 are turned on and all the transistors N2 are turned off. The first through fourth unit charge pumps 1A through 1D are transformed into diodes D. The resultant capacitance is C/4. The capacitance is reduced in the condition of FIG. 4A. The supply power source VDD is transferred to the output terminal Z through the diodes D and Dz. The capacitor CL is a load capacitor.

FIG. 4B can be regarded as an equivalent circuit of FIG. 3 in the condition that the transistor N1 is turned on and the transistor N2 is turned off between the first and second charge pumps 1A and 1B, the transistor N1 is turned on and the transistor N2 is turned off between the third and fourth unit charge pumps 1C and 1D, and the transistor N1 is turned off and the transistor N2 is turned on between the second and third unit charge pumps 1B and 1C.

FIG. 5 is a detailed circuit diagram of the level shift circuit of FIG. 3. The outputs KOUT and KOUTB which are inverted from each other are generated according to an output S4 of the auxiliary charge pump circuit 4 and control signals S1, S2 and S3. The output S4 of the auxiliary charge pump circuit 4 is maintained to be in a high voltage condition. Therefore, if the control signal S1, S2 or S3 is "HIGH", the output of an invert gate G1 becomes "LOW", whereby a transistor Q6 is turned off and a transistor Q5 is turned on. At this time, since transistors Q3 and Q4 are in the condition of turn on, a transistor Q2 is turned on while a transistor Q1 is turned off. Therefore, the output KOUT becomes "HIGH" and the output KOUTB becomes "LOW".

FIG. 6A is a graph for comparing an output(X) of the conventional charge pump circuit and an output(Y) of the charge pump circuit of the present invention.

As shown in FIG. 6A, the conventional charge pump circuit takes much time to rise up to VCC voltage since charge pumping starts at a voltage far lower than VCC voltage.

However, as shown in FIG. 6B, the present invention increases the capacitance by parallely connecting the first through fourth unit charge pump 1A through 1D at the beginning(STEP 1) of pumping operation, and decreases the capacitance by serially connecting the first and second unit charge pumps 1A and 1B, serially connecting the third and fourth unit charge pumps 1C and 1D, and connecting the outputs of the second and fourth unit charge pumps 1B and 1D to the output terminal Z as shown in step 2. At the final step(STEP 3), the first through fourth unit charge pumps 1A through 1D are serially connected as shown in FIG. 1. Therefore, as shown in FIG. 6A, since the pumping operation starts at about 2.2V, the pumping time is reduced as well as the power consumption is reduced.

As described above, the present invention has an excellent effect that the charge transfer efficiency is increased at the initial operation of the charge pump circuit as well as the programming time can be reduced at the time of programming flash memory devices utilizing high voltage.

The foregoing description, although described in its preferred embodiment with a certain degree of particularity, is only illustrative of the principle of the present invention. It is to be understood that the present invention is not to be

limited to the pref rred embodiments disclosed and illustrated herein. Accordingly, all expedient variations that may be made within the scope and spirit of the present invention are to be encompassed as further embodiments of the present invention.

What is claimed is:

1. A charge pump circuit comprising:

a first unit charge pump connected to a supply power source and performing a pumping operation according to clock signals;

a second unit charge pump connected to said supply power source and performing a pumping operation according to said clock signals; and

a serial and parallel switching circuit for selectively transferring an output of said first unit charge pump to an input or output of said second unit charge pump according to a control signal.

2. The charge pump circuit as claimed in Claim 1, wherein said serial and parallel switching circuit comprises a first switching means for connecting an output of said first unit charge pump to an input of said second charge pump, and a second switching means for connecting said output of said first unit charge pump to said output of said second unit charge pump.

3. The charge pump circuit as claimed in Claim 1, further comprising:

an auxiliary pumping circuit performing a pumping operation according to said clock signals to control said serial and parallel switching circuit; and

a level shift circuit generating two output signal, which are inverted from each other, according to said output of said auxiliary pumping circuit and other control signal.

4. A charge pump circuit comprising:

a plurality of unit charge pump connected between a supply power source and an output terminal and performing a pumping operation according to clock signals; and

a plurality of serial and parallel switching circuits for selectively transferring each output of said unit charge pump to an input of next unit charge pump said output terminal according to control signals.

5. The charge pump circuit as claimed in Claim 4, wherein said serial and parallel switching circuit comprises:

a first switching means for connecting said input and output of said unit charge pumps according to said control signals; and

a second switching means for connecting said output of each said unit charge pump to said output terminal according to said control signals.

6. A charge pump circuit as claimed in Claim 1, further comprising:

an auxiliary pumping circuit performing a pumping operation according to said clock signals to control said serial and parallel switching circuit; and

a level shift circuit generating two output signal, which are inverted from each other, according to said output of said auxiliary pumping circuit and other control signal.

The Patent Office

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Application No: GB 9526040.2 **Examiner:** Brian Ede
Claims searched: 1-6 **Date of search:** 8 March 1996

Patents Act 1977
Search Report under Section 17

Databases searched:

UK Patent Office collections, including GB, EP, WO & US patent specifications, in:

UK Cl (Ed.O): H2F(FCP,FXT,FXX) G3U(UAA3,UAA9) G4C(C11407P,C1606S)

Int Cl (Ed.6): HO2M 3/07 G05F 3/20 G11C 5/14 11/407 16/06

Other: Online: WPI

Documents considered to be relevant:

Category	Identity of document and relevant passage	Relevant to claims
A	GB 2245112 A (PHILIPS) whole document relevant	1 and 4
A	GB 1364618 (KK DAINI SEIKOSHA) see Fig 3	1 and 4
X	US 5237209 (ANALOG DEVICES INC) see K1-K3 24b and 26b Fig 1	1 and 4 at least .

X	Document indicating lack of novelty or inventive step	A	Document indicating technological background and/or state of the art.
Y	Document indicating lack of inventive step if combined with one or more other documents of same category.	P	Document published on or after the declared priority date but before the filing date of this invention.
&	Member of the same patent family	E	Patent document published on or after, but with priority date earlier than, the filing date of this application.